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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sinclair et al.	Examiner:	Harold Kim
Serial No.	09/325,882	Art Group:	2182
Filing Date:	June 4, 1999	Our file no.	00100.99.0039
Confirmation No.	3412	Docket No.	0100.9900390

Title: **POWER REDUCTION CIRCUIT AND METHOD WITH MULTI CLOCK BRANCH CONTROL**

Box Fee Amendment
Assistant Commissioner for Patents
U.S. Patent and Trademark Office
Washington, D.C. 20231

Attn: Examiner Harold Kim

Certificate of First Class Mailing

I hereby certify that this paper is being sent via first class mail to: Box Fee Amendment, Assistant Comm. For Patents, U.S. Patent & Trademark Office, Washington, D.C. 20231 on this date.

1-28-03 Karenina Oliver
Date: *Karenina Oliver*

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AMENDMENT AND RESPONSE

Dear Sir:

Applicants respectfully submit the following Amendment in response to the Action mailed October 9, 2002.

IN THE SPECIFICATION

Please replace the paragraph beginning at page 2, line 16 with the following rewritten paragraph:

C1

A problem arises with such devices since power consumption and thermal dissipation needs to be minimized for portable devices without unnecessarily sacrificing operational performance. Also, the same problem arises for non-portable devices due to increased circuit density and increased clock speeds. The power dissipation of a graphics controller chip and other integrated circuits are typically related to the operational activity of memory. Conventional portable display systems typically have power management systems that generate system level standby/suspend commands. During system level standby/suspend modes, graphics controller subsystems and other subsystems may typically respond by forcing the frame buffer memory